MP0069

APPLICATION

FOR

UNITED STATES LETTERS PATENT

Be it known that we, Zining Wu, citizen of the People's Republic of China and Gregory Burd, citizen of the United States of America, have invented new and useful improvements in:

PARITY CHECK MATRIX AND METHOD OF FORMING THEREOF

of which the following is the specification.

PARITY CHECK MATRIX AND METHOD OF FORMING THEREOF

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Gregory Burd

CROSS REFERENCE TO RELATED APPLICATIONS

The present invention claims priority under 35 U.S.C. §119 (e) from U.S. provisional application serial no. 60/214781, entitled "Address Generator for LDPC Encoder and Decoder and Method Thereof," filed June 28, 2000, the contents of which are incorporated herein by reference.

The present invention is related to the following commonly-assigned, copending applications:

"Multi-Mode Iterative Detector", filed on April 27, 2000 and assigned application Serial No. 09/559186, the contents of which are incorporated herein by reference,

"LDPC Encoder and Method Thereof", filed on even date and assigned application Serial No. _____ (Attorney Docket No. MP0064), the contents of which are incorporated herein by reference,

"LDPC Decoder and Method Thereof", filed on even date and assigned application Serial No. _____ (Attorney Docket No. MP0065), the contents of which are incorporated herein by reference, and

"Address Generator for LDPC Encoder and Decoder and Method Thereof" filed on even date and assigned application Serial No. _____ (Attorney Docket No. MP0063), the contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to a parity check matrix for a linear block encoder and decoder in a data transmission system. More particularly, the present invention relates to a parity check matrix and method of forming thereof for a

low-density parity-check code (LDPC) encoder for a write channel and decoder for a read channel in a disk drive system.

Description of the Related Art

Figs. 1 and 2 illustrate data transmission systems each employing a linear block code encoder on the transmission side and a soft linear block code decoder on the receiver side. The linear block code utilized in various systems includes a low-density parity-check (LDPC) code.

With either system, the parity check matrix is an important element in a low-density parity-check (LDPC) code. The parity check matrix effects system performance in terms of computation efficiency, accuracy and reliability. A linear code is a set of codewords, **x**, satisfying the matrix equation (1)

$$\mathbf{H} \bullet \mathbf{x} = 0 \qquad (1),$$

where **H** is an **M** x **N** matrix, and **x** is a 1 x N vector.

The parity check matrix for an LDPC encoder/decoder is sparse, that is a small portion of the elements being one, all other elements being zero. An example of a parity check matrix is shown in equation 2 that corresponds to the factor graph shown in Fig. 3.

$$H = \begin{bmatrix} 1011 \\ 0111 \end{bmatrix} \qquad (2)$$

which defines the following parity-check equations for the codeword **x**

$$x1+x3+x4=0$$

$$x2+x3+x4=0$$

Fig. 3 is a factor graph of the parity matrix of equation 2. The factor graph contains two types of nodes the bit node (*e.g.* b1, b2, b3, and b4) and the check nodes (e.g. e1, e2). Each bit node corresponds to a bit in the codeword, and each check node represents a parity-check equation (*i.e.,* a row in the parity check matrix **H**). Hence, the factor graph for an LDPC code with an **M** x **N** parity check matrix **H** contains **M** check nodes and **N** bit nodes. An edge between a check node and a bit node exists if and only if the bit participates in the parity-check equation represented by the check

node. The factor graph shown in Fig. 3 is "bipartite" in which the nodes can be separated to two groups, namely check nodes and bit nodes. Connections are allowed only between nodes in different groups.

A cycle in a factor graph refers to a finite set of connected edges that start and end at the same node. The bold lines in Fig. 3 represent a cycle length of four. As can be appreciated by one of ordinary skill in the art, four is the shortest cycle length a parity check matrix can have. The inventors have observed that the existence of period-4 cycles causes degradation in performance of sum-product decoding algorithms. The sum-product algorithm is discussed by Zining Wu in *Coding and Iterative Detection For Magnetic Recording Channels,* 2000, Kluwer Academic Publishers, pages 55-60, the contents of which are incorporated by reference.

One example of a conventional parity-check is the simple parity-check (SPC) matrix. The simple parity check matrix is shown in Öberg, Mats and Siegel, Paul, *Parity Check codes For Partial Response Channels*, I.E.E.E. Global Telecommunications Conference – Globalcom '99, pages 717-722, 1999.

The SPC matrix is defined by two parameters, N and M, denoting the coded block length and the number of check equations, respectively. An example of an SPC matrix is shown in equation 4.

$$SPC(N,M) = \begin{bmatrix} 11...100.....0 \\ 00...011...100...0 \\ ..... \\ ..... \\ 0.....11...1 \end{bmatrix} \begin{matrix} \\ \\ \\ \\ \\ \end{matrix} \text{M} \qquad (4)$$

N

The factor graph corresponding to this parity check matrix does not contain any cycles. This matrix also has a column weight tc =1. Column weight tc refers to the number of "1"s in each column. Since the complexity of the sum-product decoding algorithm increases linearly with tc, it is desirable to have a small tc. The minimum Hamming distance dmin=2 for the SPC matrix of equation (4). The Hamming distance is the minimum number of columns that are linearly dependent in the parity check matrix. A large dmin insures large separation between codewords, which results in a low bit error rate (BER). However the coding gain of the SPC matrix of equation (4) is limited since dmin=2. The code rate for the SPC matrix is 1-M/N.

Another conventional example of a parity check matrix is the interleaved parity check matrix in which additional parity-check equations are added to the SPC matrix in an interleaved way to increase the dmin. As shown in equation 5, an IPC matrix consists of two parts, the top part which is similar to an SPC matrix and the bottom part in which each row has the same number of "1"'s. The IPC matrix can be specified by one parameter P, which is the number of "1"'s in each row. This matrix has a dimension of $2PxP^2$. The coded block length is P^2 and the number of parity-check equations are 2P.

$$IPC(3) = \begin{bmatrix} 111000000 \\ 000111000 \\ 000000111 \\ \text{--------} \\ 100100100 \\ 010010010 \\ 001001001 \end{bmatrix} \qquad (5)$$

The IPC matrix does not contain any period-4 cycles, has a dmin=4 and tc=2. As is understood by one of ordinary skill in the art, there are only 2P-1 independent rows in the parity check matrix. The code rate for the IPC matrix is $(P^2-2P+1)/P^2$.

One construction of a D6 parity check matrix is shown in equation 6. Its basis is an IPC matrix having P as an even number. Its has a dimension of (3P-1) x P(P-1).

$$(4) = \begin{bmatrix} 111100000000 \\ 000011110000 \\ 000000001111 \\ 100010001000 \\ 010001000100 \\ 001000100010 \\ 000100010001 \\ \text{----------} \\ 100001000010 \\ 010000100001 \\ 001000010000 \\ 000100001000 \end{bmatrix} \text{IPC} \qquad (6)$$

Added Parity

The upper part contains 2P-1 rows and the bottom part contains P rows where the "1"'s are arranged diagonally with a shift of one column between each block. To obtain a Hamming distance of 6, then P-1, P and P+1 are relatively prime to each other. This matrix has a dmin =6, there is no cycle for period, tc= 3-(1/(p+1)) or ≈3, and a code rate of $(P^2-4P+2)/(P^2-P)$.

Summary of the Invention

According to a first aspect of the invention, a data transmission system is provided for transmitting user data to and receiving data from a communication channel, comprising a parity check matrix having M tiers, wherein M≥2, Dmin = 2 * M for M=1..3 or 2*M ≥ Dmin ≥ 6 for M > 3, wherein Dmin is the minimum Hamming distance, tc=M, wherein tc is the column weight, and cycle-4=0. A linear block encoder encodes the user data in response to the parity check matrix, and a transmitter transmits an output of the linear block encoder to the communication channel. A soft channel decoder decodes data, and a soft linear block code decoder to decode data decoded by the soft channel decoder in response to the parity check matrix.

According to a second aspect of the present invention, a parity check matrix is provided for one of a low-density parity-check encoder and a low-density parity-check decoder. The comprises M tiers, wherein M≥2, Dmin = 2 * M for M=1..3 or 2*M ≥ Dmin ≥ 6 for M > 3, wherein Dmin is the minimum Hamming distance, tc=M, wherein tc is the column weight, and cycle-4=0.

According to a third aspect of the present invention, each of the M tiers comprises an identity matrix having a corresponding rank P_i, wherein $1 \leq i \leq M$.

According to a fourth aspect of the present invention, the rank of the identity matrix of one of the tiers is mutually prime with respect to the rank of the identity matrix of another one of the tiers.

According to a fifth aspect of the present invention, the M tiers are arranged in increasing rank order.

According to a sixth aspect of the present invention, the matrix comprises C columns, wherein $C \leq P_1 * P_2$.

According to a seventh aspect of the present invention, the matrix comprises R rows, wherein $R=\sum_{i=1}^{M} P_i$.

According to an eighth aspect of the present invention, the matrix comprises $\sum_{i=1}^{M} P_i - (M-1)$ independent rows.

According to a ninth aspect of the present invention, the matrix comprises $\sum_{i=1}^{M} P_i - (M-1)$ parity bits.

According to a tenth aspect of the present invention, the matrix comprises $P_1 \times P_2 - \sum_{i=1}^{M} P_i + (M-1)$ maximum user bits.

According to an eleventh third aspect of the present invention, for each element

$$[A_{r,c}]$$

$$For \sum_{j=1}^{n-1} P_j + 1 \le r \le \sum_{j=1}^{n} P_j,$$

$$A_{r,c} = \left\{ \begin{array}{l} 1, if c \bmod(P_n) = r - \sum_{j=1}^{n-1} P_j \\ 0, otherwise \end{array} \right\}$$

$$0 \le c \le C$$

$$C \le P_1 * P_2$$

According to a twelfth aspect of the present invention, M=3, the number of rows = $P_1+P_2+P_3$, the number of columns= P1 * P2, dmin=6, and tc=3.

According to a thirteenth aspect of the present invention, a code rate = $(P_1 P_2+P_1-P_2-P_3+2)/(P_1 P_2)$.

According to a fourteenth aspect of the present invention, a data transmission system is provided for transmitting user data to and receiving data from a communication channel, comprising a parity check matrix having M tiers, M≥2, Dmin = 2 * M for M=1..3 or 2*M ≥ Dmin ≥ 6 for M > 3, wherein Dmin is the minimum Hamming distance, tc=M, wherein tc is the column weight, and cycle-4=0. Linear block encoding means encodes the user data in response to the parity check matrix. Transmitting means transmits an output of the linear block encoding means to the communication channel, and soft channel decoding means decodes data. Soft linear

block code decoding means decodes data decoded by the soft channel decoding means in response to the parity check matrix.

According to a fifteenth aspect of the present invention, a method is provided for transmitting data to and receiving data from a communication channel, comprising the steps of:

(a) generating a parity check matrix comprising:

M tiers, wherein M≥2,

Dmin = 2 * M for M=1..3 or 2*M ≥ Dmin ≥ 6 for M > 3, wherein Dmin is the minimum Hamming distance,

tc=M, wherein tc is the column weight, and

cycle-4=0;

(b) linear block encoding the data in accordance with the parity check matrix generated in step (a);

(c) transmitting the data encoded in step (b) to the communication channel;

(d) receiving the data from to the communication channel;

(e) soft channel decoding the data read in step (d) in accordance with data decoded in step (g);

(f) generating an address in accordance with the data soft linear block code decoding the data decoded in step (e); and

soft linear block code decoding data decoded by in step (e) in accordance with the address generated in step(f).

According to a sixteenth aspect of the present invention, a computer program embodied in a medium is provided for transmitting data to and receiving data from a communication channel, comprising the steps of:

(a) generating a parity check matrix comprising:

M tiers, wherein M≥2,

Dmin = 2 * M for M=1..3 or 2*M ≥ Dmin ≥ 6 for M > 3, wherein Dmin is the minimum Hamming distance,

tc=M, wherein tc is the column weight, and

cycle-4=0;

(b) linear block encoding the data in accordance with the parity check matrix generated in step (a);

(c) transmitting the data encoded in step (b) to the communication channel;

(d) receiving the data from to the communication channel;

(e) soft channel decoding the data read in step (d) in accordance with data decoded in step (g);

(f) generating an address in accordance with the data soft linear block code decoding the data decoded in step (e); and

soft linear block code decoding data decoded by in step (e) in accordance with the address generated in step(f).

Other objects and attainments together with a fuller understanding of the invention will become apparent and appreciated by referring to the following description and claims taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

In the drawings wherein like reference symbols refer to like parts.

Fig. 1 is a block diagram of a data transmission system;

Fig. 1A is a block diagram of a generalized data transmission system

Fig. 2 is a block diagram of an alternate data transmission system;

Fig. 3 is an example of a factor graph;

Fig. 4 is an example of a parity check matrix in accordance with the present invention; and

Fig. 5 is another example of a parity check matrix in accordance with the present invention.

Description of the Preferred Embodiments

Fig. 1A is a block diagram of a generalized data transmission system. The generalized data transmission system comprises a linear block code encoder 110, a communication channel 120 and a linear block code decoder 130. The operation of the

generalized will now be discussed. Input data is encoded by linear block code encoder 110, which generates parity data in a known manner utilizing linear block codes. One example of a linear block code is a low-density parity-check (LDPC) which is discussed by Robert G. Gallager in *Low-Density Parity-Check Codes*, 1963, M.I.T. Press and by Zining Wu in *Coding and Iterative Detection For Magnetic Recording Channels,* 2000, Kluwer Academic Publishers, the contents of each of which are incorporated in their entirety by reference. The data is then transmitted over communication channel 120. The data from communication channel 120 is then decoded by linear block code decoder 130 in a known manner.

Referring now to Fig. 1, which illustrates a more detailed conventional digital data transmission system. As shown therein, a digital data transmission system comprises a transmitting section 300 for transmitting user data to receiver 500 via communication channel 401.

The operation of transmission section 300 will now be explained. Prior to processing by transmitting section 300, input or user data maybe encoded with an error correcting code, such as the Reed/Solomon code, or run length limited code (RLL) or a combination thereof by encoder 302. The encoded output by encoder 302 is then deinterleaved by deinterleaver 308 for input to linear block code encoder 304 which generates parity data in a known manner utilizing linear block codes. Deinterleaver 308 permutes the data so that the same data is reordered before encoding by linear block code encoder 304. By permuting or redistributing the data, deinterleaver 308 attempts to reduce the number of nearest neighbors of small distance error events, when the channel contains intersymbol interference. User data at the output of encoder 302 is referred to as being in the channel domain; that is the order in which data is transmitted through the channel. The order of data processed by deinterleaver 308 is referred to as being in the linear block code domain. The parity data from linear block code encoder 304 is combined with the data encoded by encoder 302 by multiplexer 306 for input to channel transmitter 310.

Transmitter 310 transmits the combined user and parity data from multiplexer 306 typically as an analog signal over communication channel 401 in the channel domain. Communication channel 401 may include any wireless, wire, optical and the like communication medium. Receiver 500 comprises an analog to digital converter 502 to convert the data transmitted on communication channel 401 to a digital signal. The digital signal is input to soft channel decoder 504, which provides probability

information of the detected data. Soft channel decoder may be implemented by a soft Viterbi detector or the like. The output of the soft channel decoder 504, which is in the channel domain, is converted into the linear block code domain by deinterleaver 510. Deinterleaver 510 is constructed similarly to deinterleaver 308. Soft linear block code decoder 506 utilizes this information and the parity bits to decode the received data. One output of soft linear block code decoder 506 is fed back to soft channel decoder 504 via interleaver 512, which converts data in the linear block code domain to the channel domain. Interleaver 512 is constructed to perform the reverse operations of deinterleaver 510. Soft channel decoder 504 and soft linear block code decoder 506 operate in an iterative manner to decode the detected data.

The other output of soft linear block code decoder 506 is converted from the linear block domain to the channel domain by interleaver 514. Interleaver 514 is constructed similarly to interleaver 512. The output of interleaver 514 is passed on for further processing to decoder 508. Decoder 508 is implemented to perform the reverse operations of encoder 302 or correct for any errors in the received data.

An alternative to incorporating deinterleaver 308 in transmission section 300 and deinterleavers 510 and 514 and interleaver 512 in receiving section 500 is to utilitize an address generator to provide an address of the appropriate equation of the linear block code encoder. The address generator is described in "Address Generator for LDPC Encoder and Decoder and Method Thereof" filed on even date and assigned application Serial No. _____ (Attorney Docket No. MP0063), the contents of which are incorporated herein by reference. As discussed therein the linear block code encoder is not dependent on a position of a bit interleaved. Rather the linear block code encoder only requires a list of equations for a given bit. In other words, there is no need to process the data in the order defined by the deinterleaver, instead data may be processed in the same order as it is written to the channel. This can be accomplished by incorporating an address generator to provide an address of the appropriate equation of the linear block code encoder. This principle can be similarly applied to the soft linear block decoder. As a result, deinterleaver 308 of the conventional system is now replaced by address generator 328, and deinterleaver 510 is now replaced by address generator 530. Accordingly, there is no requirement for the physical interleaving of data in the receiver 500', since the data remains in the same order as the order of bits of data in the channel throughout this system. The order of bits of data transmitted through the channel is referred to as the channel domain.

The linear block code encoder in Figs. 1, 1A and 2 utilize a parity check matrix to generate the parity data. The parity check matrix in a low-density parity-check code, in accordance with the present invention, comprises no period-4 cycles. Period 4 cycles cause degradation in performance of the sum-product algorithm. Additionally, the parity check matrix comprises a large dmin or minimum Hamming distance of the code. This refers to the minimum number of columns that are linearly dependent in the parity check matrix. A large dmin insures separation between codewords to provide a low bit error rate. Another parameter tc is the number of "1"'s in each column of the parity check matrix. Since the complexity of the sum-product decoding algorithm increases linearly with tc, the parity check matrix preferably has a small tc.

The parity check matrix in accordance with the present invention is shown in equation 7.

$$\begin{bmatrix} I_{p1,1}I_{P1,2}\ldots I_{P1,r} \\ I_{p2,1}I_{P2,2}\ldots I_{P2,r}* \\ I_{p3,1}I_{P3,2}\ldots I_{P3,r}* \\ . \quad . \quad .... \\ I_{pM,1}I_{PM,2}\ldots I_{PM,r}* \end{bmatrix} \qquad (7)$$

In equation 7, I_{Pi} denotes a P_i x P_i (rank P_i) identity matrix for i= 1 to M.

Equation 8 shows an identity matrix with a rank of 4.

$$\begin{bmatrix} 1000 \\ 0100 \\ 0010 \\ 0001 \end{bmatrix} \qquad (8)$$

The parity matrix can be generalized as comprising M tiers (M≥2), each tier i comprising a row of identity matrixes I_{Pi} of rank P_i. The matrix is arranged such that $P_1 < \ldots < Pi < \ldots < P_M$ and P1, Pi, P_M are mutually prime. The number of columns in the preferred matrix is less than or equal to (P_1 x P_2). As can be readily seen, for tiers greater than 2, the last matrix in each row is not complete. Equation 8A is illustrative of a partial identity matrix of rank 4

$$\begin{bmatrix} 100 \\ 010 \\ 001 \\ 000 \end{bmatrix} \qquad (8A)$$

More specifically, each element $A_{r,c}$, for row r and column c, is as follows:

$$For \sum_{j=1}^{n-1} P_j + 1 \le r \le \sum_{j=1}^{n} P_j,$$

$$A_{r,c} = \left\{ \begin{array}{l} 1, if c \bmod(P_n) = r - \sum_{j=1}^{n-1} P_j \\ 0, otherwise \end{array} \right\}$$

$$0 \le c \le C$$

$$C \le P_1 * P_2$$

The parity matrix in accordance with the preferred embodiment of the present invention comprises a total of $\sum_{i=1}^{M} P_i$ rows in the matrix, of which $\sum_{i=1}^{M} P_i - (M-1)$ rows are independent. Thus the total number of parity bits is $\sum_{i=1}^{M} P_i - (M-1)$, and the maximum number of user bits is $P_1 \times P_2 - \sum_{i=1}^{M} P_i + (M-1)$. To accommodate a smaller sector size, the columns of the parity check matrix can be truncated. As such the number of user bits are reduced, while the number of parity bits and dmin remain the same. The preferred matrix in accordance with present invention comprises M tiers, Dmin=2M for M=1..3 or 2*M ≥ Dmin ≥ 6 for M > 3, tc=M and cycle-4 = 0.

For M=3, the matrix has a dimension of (P_1+P_2+P_3) x (P_1P_2), dmin=6 and tc=3. The code rate for the matrix = (P_1P_2- P_1-P2-P3+2)/ (P_1P_2).

Reference is now made to Fig. 4, which shows a parity check matrix in accordance with the preferred embodiment of the present invention. The parity check matrix comprises 222 rows (or equations) by 5402 columns, which comprises 220 linearly independent rows (where 5402 =73*74). The matrix can be divided into three

tiers of equations having 73, 74 and 75 equations, respectively. As can be seen the tiers (73, 74 and 75) are mutually prime. The set of independent rows can be obtained by canceling the last row of the second tier and third tier, namely the 147th row and the 222nd row. The following table shows the values of the elements in the matrix:

Tier	i^{th} position	i^{th} position
1	1 if r = i(mod73)	0 if r ≠ i(mod73)
2	1 if r = i(mod74)	0 if r≠ i(mod74)
3	1 if r = i(mod75)	0 if r ≠ i(mod75)

Where r is the index within a tier.

A matrix having 5402 columns can process a maximum LDPC codeword of 5402 bits. Of course, as will be appreciated by one of ordinary skill in the art, the matrix may be truncated to accommodate a smaller block, however the matrix must be at least 222 x 4366. (The minimum size is dependent on the RLL encoding.) The preferred matrix contains no cycles, since a matrix having cycles has degraded performance that degrades exponentially. The Dmin can be determined as follows. With the first tier only, the parity check matrix has a $D_{min}=2$; by adding the second tier, the parity check matrix has a $D_{min}=4$; and by adding the third tier, the parity check matrix has a $D_{min}=6$. This matrix does not to contain any period-4 cycles.

Reference is now made to Fig. 5, which shows an alternate parity check matrix in accordance with the preferred embodiment of the present invention. Similar to the previous parity check matrix, this parity check matrix comprises 222 rows (or equations) by 5402 columns, which comprises 220 linearly independent rows (where 5402 =73*74). The matrix can be divided into three tiers of equations having 73, 74 and 75 equations, respectively. As can be seen the tiers (73, 74 and 75) are mutually prime. The set of independent rows can be obtained by canceling the last row of the second tier and third tier, namely the 147th row and the 222nd row. The following table shows the values of the elements in the matrix:

Tier	i^{th} position	i^{th} position
1	1 if r = floor (i/73)	0 if r ≠ floor (i/73)
2	1 if r = i(mod74)	0 if r≠ i(mod74)
3	1 if r = i(mod75)	0 if r ≠ i(mod75)

Where r is the index within a tier.

While the invention has been described in conjunction with several specific embodiments, it is evident to those skilled in the art that many further alternatives, modifications and variations will be apparent in light of the foregoing description. More specifically, it is apparent that various matrix manipulations may be performed on the preferred matrix, which results in an equivalent. Such manipulated matrix falls with spirit and scope of the claims. While the present invention maybe implemented as an integrated circuit, it is contemplated that the present invention may also be implemented as discrete components or a general-purpose processor operated in accordance with program code instructions or computer program or combination thereof. These program code instructions can be obtain from a medium, such as network, local area network, the Internet, or storage devices. Such storage devices include, by way of example, magnetic storage devices, optical storage devices, electronic storage devices, magneto-optical device and the like. Thus, the invention described herein is intended to embrace all such alternatives, modifications, applications and variations as may fall within the spirit and scope of the appended claims.